A 250 µm x 12.5 µm rectangular pixel with resistive poly gate for line scan CMOS image sensor

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***Abstract* — This paper presents a 250 µm × 12.5 µm rectangular pixel using the resistive poly gate. This pixel enables a linear potential gradient along the gate, which modulates the buried channel beneath it, thus, establishing a continuous drift field spanning the photodiode's entire length. During integration, photogenerated charges first move into the buried channel and then transfer along the buried channel via the resistive gate induced drift field. Charge transfer time measurement demonstrates that the proposed pixel structure achieves sub-3 µs charge transfer performance, validating its capability to meet the requirements in high-speed, long-pitch sensor applications of line-scan imaging.**

I. INTRODUCTION

In this paper, a 250 µm × 12.5 µm rectangular pixel has been developed for a variety of applications, such as displacement sensors, spectrometers, optical coherence tomography (OCT), etc. Typically, in the case of such long pixels, if the charge transfer is dominant by diffusion, the charge transfer time scales quadratically with pixel length. This would significantly limit the sensor frame rate.

To improve the charge transfer speed in large photodiode, several techniques have been studied, such as geometric shaping, graded doping, or tilt angle optimization of the photodiode n-well implant [1-8]. However, the electric field achieved by adopting these methods is at the cost of a reduced diode fill factor or additional fabrication steps, which increase the design complexity and cost.

To address this limitation, we introduce a partially pinned photodiode (PPPD) structure incorporating a resistive poly gate [9] integrated with a CMOS image sensor (CIS) process. Experiment shows that such a structure enables a short charge transfer time with low image lag performance. Compared to a CCD or CMOS TDI area image sensor which is used as a linear sensor by line binning, such line scan CIS offers higher speed transfer of charges.

II. PIXEL STRUCTURE

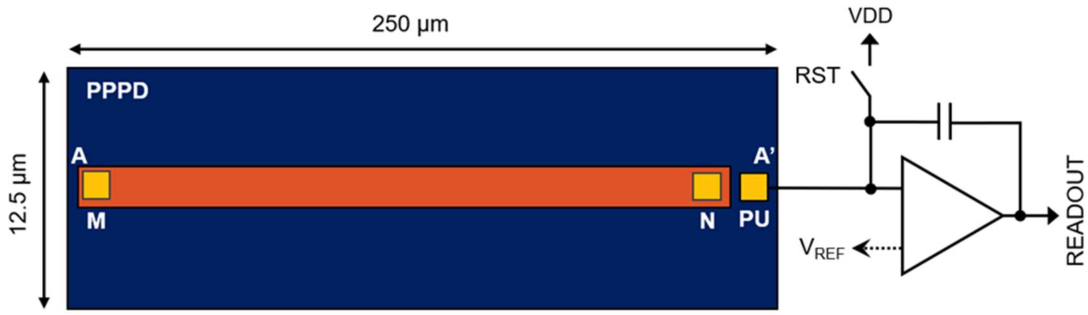
As shown in Fig. 1 (a) and (b), to generate a uniform-distributed lateral electric field in the direction from A to A', the proposed partially pinned photodiode (PPPD) employs a resistive polysilicon gate positioned centrally on the photodiode region. This gate structure operates as a tunable voltage divider. By applying a voltage difference across the resistive gate at node M (the voltage level is marked as TXL, a lower voltage level) and N (the voltage level is marked as TXH, a higher voltage level), a linear electrostatic potential gradient is induced across the gate's length, as shown in Fig. 1 (c). This gradient, in turn, modulates the buried channel beneath the gate, creating a drift field that spans the entire photodiode length. During the exposure time, the signal charges that are collected at the photodiode initially move to the buried channel, and then transfer along the channel towards the pick-up (PU) point. This transportation mechanism enables the charges to undergo drift instead of diffusion, ensuring short charge transfer time even in the elongated 250 µm pixel.

A capacitive trans-impedance amplifier (CTIA) is connected to the photodiode for signal readout, as well as signal amplification and noise reduction.

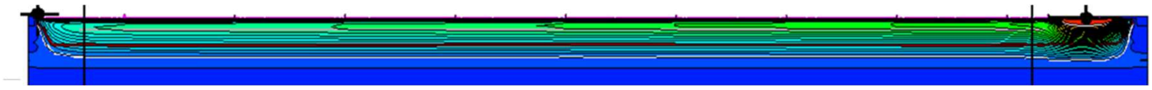
III. CHARACTERIZATION RESULTS

To evaluate the performance of the proposed pixel, a 512-column linear CMOS image sensor device has been designed and fabricated. To characterize the operation of the resistive gate PPPD pixel, a laser-microscope setup incorporating high-resolution XYZ mechanical has been designed and assembled (Fig. 2a). The setup uses 640 nm laser focused into the device under test (DUT) surface via a long working distance (LWD) objective, achieving a laser spot size smaller than 5 µm (Fig. 2b). The laser pulse temporal position is synced with DUT control signals and the pulse width can be varied across 0.1-100 µs range.

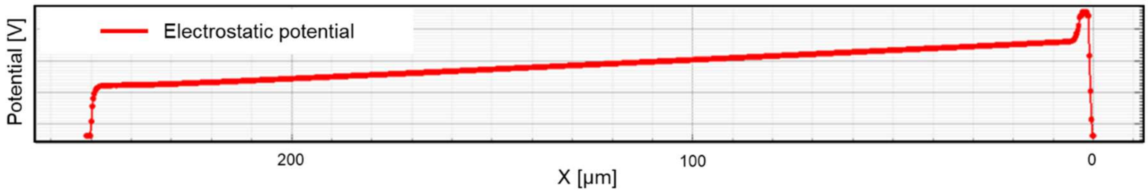
To evaluate the performance of the resistive gate concept, so-called charge transfer time measurement is proposed.



(a)



(b)

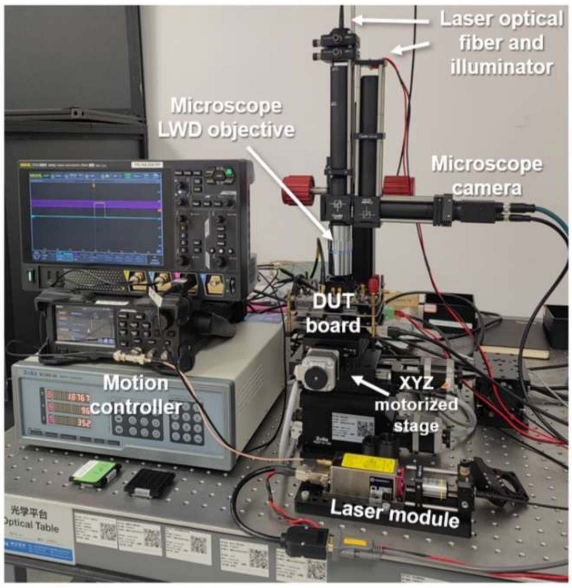


(c)

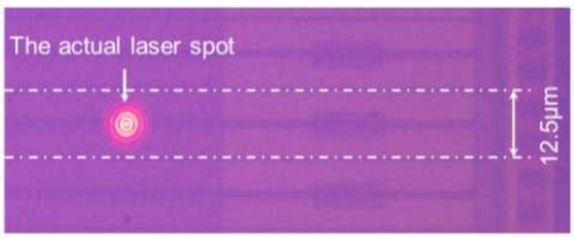
Fig. 1 (a) Schematic outline of the PPPD structure with resistive gate and its simplified readout circuit; (b) A-A' cross-section of the PPPD structure; (c) Electro potential along the cross-section

In this measurement, pixel response is sampled when the illumination pulse is swept from before and during the integration time period. Thus, the part of pixel response, when RST is still high, gives an idea of how long it takes to empty the photodiode. We define this period as charge transfer time, as shown in Fig. 3. Fig. 4 shows a typical example of pixel response to light pulse temporal position sweep. The pixel response under different TXH as a function of the light pulse temporal position is plotted in Fig. 5. It can be observed that the charge transfer time is inversely proportional to the voltage difference between TXH-TXL. A two-dimensional plot of the photodiode charge transfer time as a function of TXH and TXL is shown in Fig. 6. In addition, in order to correlate the transfer time with respect to charge transfer distance along the photodiode, the laser spot has been used as the light source to illuminate different positions on the pixel. The resulting data are presented in Fig. 7.

Beyond photodiode charge transfer performance, the sensor's additional specs are evaluated. The pixel demonstrates a full well capacity (FWC) of 2.8 Me- and a maximum signal-to-noise ratio (SNR) of 71 dB. This pixel, which maintains the standard photodiode n-implant geometry and incorporates backside illumination (BSI)



(a)



(b)

Fig. 2 Charge transfer (a) measurement setup; (b) laser spot illuminating DUT pixel as seen in the microscope.

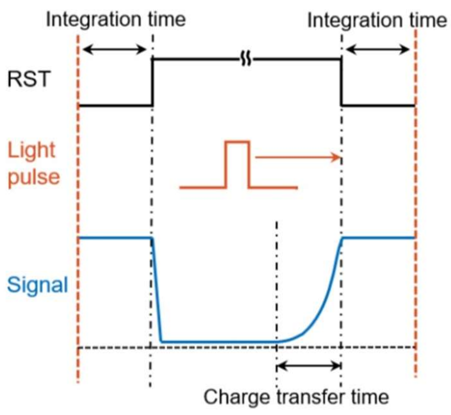


Fig. 3 measurement method timing principle.

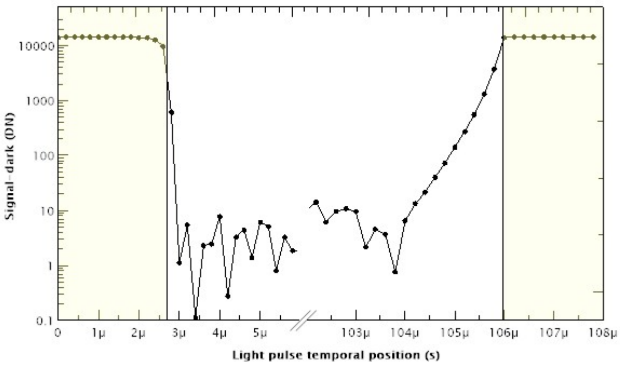


Fig. 4 Pixel response to the light pulse sweep across the 1st integration time period (yellow-shaded), RST high period and the 2nd integration time period (yellow-shaded).

processing, achieves a peak quantum efficiency (QE) of 95% and around 50% efficiency at 650 nm.

IV. Noise and Dark Current Reduction

The aforementioned resistive poly gate and PPPD pixel structure integrate with a CTIA scheme to achieve high FWC, though this combination results in a high noise level. On the other hand, when the PPPD electrostatic potential slope is always formed during long integration time, dark current (DC) is an issue.

To overcome these limitations, we propose an enhanced pixel structure that retains the resistive poly gate while combining with a fully pinned photodiode (PPD), two transfer gates (TG1 and TG2), and floating diffusion (FD) for the charge-to-voltage conversion, as shown in Fig. 8. This design facilitates the pixel operated with correlated double sampling (CDS) mode, effectively reducing reset noise. Furthermore, compared to the "PPPD + CTIA" configuration, this architecture can support a higher conversion gain (CG) through a reduced FD capacitance

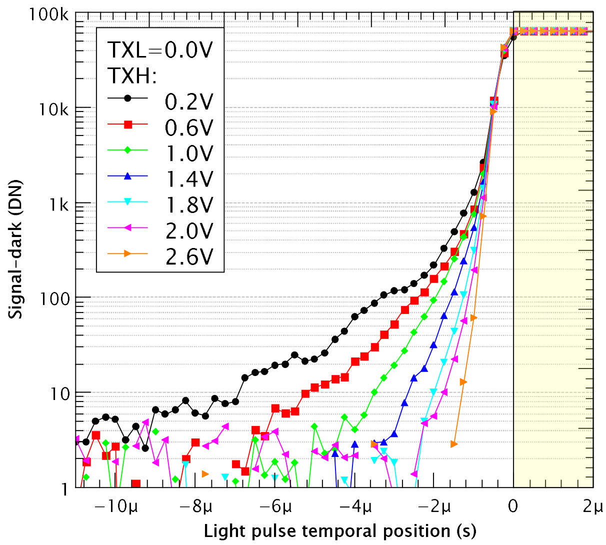


Fig. 5 Pixel response vs light pulse temporal position for various TXH values. Yellow-shaded regions indicate integration time period, all other times correspond to RST-high-period respectively.

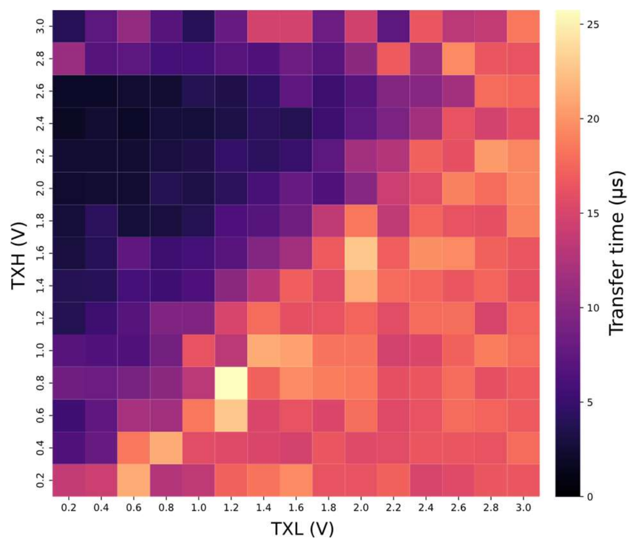


Fig. 6 Charge transfer time as function of TXH and TXL voltages.

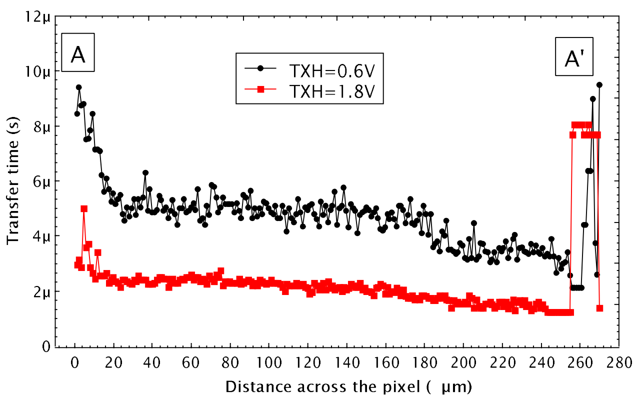


Fig. 7 Charge transfer time as a function of light spot position along the photodiode A-A'.

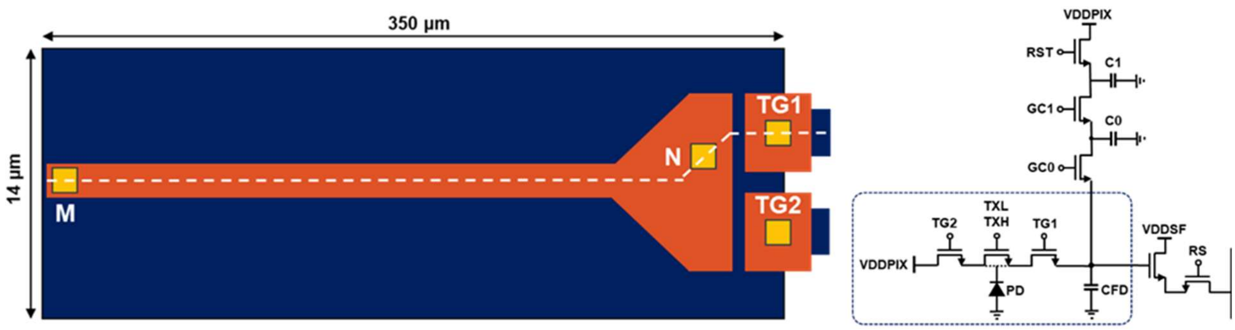


Fig. 8 Schematic of the PPD structure with resistive gate and its pixel readout circuit.

design, thereby achieving a significant noise reduction.

To suppress the DC, the pixel can be operated with the multi-pinned phase (MPP) mode [10], where the voltage at node N is dynamically adjusted during the integration and readout phases. During integration, the buried channel is maintained in a pinned state, effectively suppressing the thermionic emission of electrons from interface traps. Upon transitioning to charge transfer, the voltage is reconfigured to establish a controlled potential gradient along the channel, enabling efficient drift-driven charge transport. This dual-phase operation reduces dark current while preserving high charge transfer efficiency.

Tab. I shows the comparison specifications between the former described “PPPD + CTIA” version (Sensor ‘A’) and “PPD + TG” version (Sensor ‘B’) described in this section.

Tab. I Sensor ‘A’ and Sensor ‘B’ specifications comparison

Item	Unit	Sensor ‘A’	Sensor ‘B’
Resolution	--	0.5 k	2 k
Pixel pitch	μm^2	250 × 12.5	350 × 14
FWC	e-	2.8 M	180 k
Noise	e-	770	1.4
Dynamic range	dB	71	94
med. DC @ 37°C	e-/s	--	4 k
Max. Line rate	Hz	9.4 k	28 k

V. CONCLUSION

This paper presents a pixel design that employs a photodiode structure with a resistive poly gate integrated into a CIS fabrication process. Measurement results show that this structure and configuration effectively enhance the charge transfer speed while maintaining other sensor specifications. In addition, this structure scalability provides a comprehensive pixel pitch selection to suit diverse line scan applications.

VI. ACKNOWLEDGMENT

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